UNITED STATES PATENT APPLICATION

FOR

DAISY CHAIN GANG TESTING

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DAISY CHAIN GANG TESTING

FIELD OF THE INVENTION

[001] The present invention relates to a method and apparatus for testing integrated circuit packages, and more particularly to a method and system for performing reliability testing of integrated circuit packages without using an automatic electrical tester.

BACKGROUND OF THE INVENTION

[002] Integrated circuits are typically packaged before they are used with other components as part of a larger electronic system. Ball grid array (BGA) packages, for example, are constructed with die mounted on a substrate, and an array of solder balls mounted on the bottom of the substrate are used to attach the package to a PC board or motherboard. In contrast, molded plastic packages use lead frames on the outer edges of the package substrate to attach the package to the PC board.

[003] In order to test the reliability of the integrated circuit packages, the packages are subjected to multiple electrical stress tests. To perform some types of tests, metallization routing is used to bridge package substrate traces, creating simple electrical "loops" between pairs of BGA balls or lead frames. These electrical loops are commonly referred to as daisy chain loops.

[004] One procedure performed on the IC package during reliability stress testing is to oppositely bias parallel connected daisy chain loops and measure

cumulative leakage between the parallel loops. Although the leakage test is a simple one, almost all stress testing performed today is done with the use of an expensive Automatic Electrical Tester (ATE) and an expensive Device Under Test (DUT) circuit board. The purpose of an ATE is to functionally test the die in the IC package and is programmable. Therefore, an ATE is both complicated and expensive.

[005] Using such a complicated and expensive tester to perform simple leakage testing and other such test is an inefficient use of resources that cost semiconductor manufacturers time and money. For example, a typical ATE may cost between $1 million to $5 million dollars. In addition, a DUT board may cost between $8,000 and $12,000 for each IC package design. Thus, it is not uncommon for a semiconductor manufacture to spend $350,000 a year for DUT boards. In addition, there is a current time factor of 4 days between the time the sample is submitted for the ATE test and the results are obtained.

[006] Accordingly, what is needed is an improved method and system for performing leakage testing on IC packages that eliminates the need to use an expensive and time-consuming ATE tester. The present invention addresses such a need.

SUMMARY OF THE INVENTION

[007] The present invention provides a method and system for testing an integrated circuit package. The integrated circuit package includes a plurality of daisy chain loops that are connected to a pair of package pads, wherein

adjacent daisy chain loops are oppositely biased. Aspects of the present invention include forming a first plurality of gangs of electrically coupled daisy chain loops having a first bias, and forming a second plurality of gangs of electrically coupled daisy chain loops having a second bias. Each one of the first plurality of gangs is individually coupled to an electrical measurement device, while the second plurality of gangs are electrically coupled in common, and the common gang is coupled to the electrical measurement device. According to the method and system disclosed herein, the electrical measurement device may be used to indicate whether there is any leakage between one or more of the first plurality of gangs and the common gang, thereby eliminating the need to use an ATE tester and a sophisticated and expensive device under test (DUT) circuit board to perform reliability tests.

[008] According to the method and system disclosed herein, the present invention significantly reduces testing costs, results in faster test turnaround times, can be used for real time testing, such as during drying of the test packages in an oven, and enables testing to be performed at sites where an ATE tester is not readily available.

BRIEF DESCRIPTION OF THE DRAWINGS

[009] FIG. 1 is a side view of the reliability testing system of the present invention.

[010] FIG. 2 is a diagram illustrating a top view of the gang testing board and electrical connections thereof.

[011] FIG. 3 is a diagram illustrating a gang testing board having four edge card connectors.

DETAILED DESCRIPTION OF THE INVENTION

[012] The present invention relates to a method and apparatus for testing IC packages. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiments and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

[013] The present invention provides a reliability testing system for testing a daisy chained IC package (hereinafter test packages) that eliminates the need to use an expensive ATE tester and device under test (DUT) circuit board to perform reliability tests, such as leakage and resistance.

[014] FIG. 1 is a side view of the reliability testing system of the present invention; and FIG. 2 is a diagram illustrating a top view of the gang testing board and electrical connections thereof. Referring to both FIGS. 1 and 2, the reliability testing system 10 is a simplified testing apparatus for performing reliability tests on a test package 18. The test package 18 includes an array of pads 11, which may be BGA balls or leads, in which pairs of the pads 11 are connected to form daisy chain loops 13. As described above, adjacent parallel

lines (columns or rows) of daisy chain loops 13 are alternately biased positive and negative.

[015] The test package 18 is mounted to a conventional test socket 20. As is well known in the art, the test socket 20 has pass-through connections 22 that allow the pads 13 of the test package 18 to connect to another device or circuit board. In a preferred embodiment of the present invention, a gang testing board 12 is provided on which the test package 18 is mounted using the test socket 20.

[016] This particular gang testing board 12 includes wire fingers 22 and at least two edge card connectors; sectioned edge card connector 14 and shorted edge card connector 16 mounted along the sides of the gang testing board 12. According to the present invention, the wire fingers 24 are coupled to the pads of the test package 18 via the test socket 20, such that multiple gangs of positively biased daisy chain loops 30 are formed and multiple gangs of negatively biased daisy chain loops 32 are formed. As shown, adjacent gangs 30 and 32 formed by the wire fingers 24 are oppositely biased.

[017] The test package 18 may be mounted on the gang testing board 12 such that the positively biased gangs 30 are electrically connected in parallel to one of the edge card connectors 14 or 16, and the negatively biased gangs 32 are electrically connected in parallel to the other edge card connector 14 or 16. The two edge card connectors 14 and 16 are coupled to an electrical measuring device 26, such as a data logger system or Kelvin ohm meter, to measure cumulative leakage between the adjacent lines of daisy chain loops 13. As an

example of the electrical measuring device 26, a 32 channel data logger may be used to test a 1413 pin ball grid array (BGA) test package.

[018] In the embodiment shown in FIG. 2, the sectioned edge card connector 14 makes an electrical connection to each one of the positively biased gangs 30, while the shorted edge card connector 16 makes an electrical connection to each one of the negatively biased gangs 32. In a preferred embodiment, the wire fingers 24 are configured such that approximately two to thirteen gangs are formed, where each gang includes approximately fifteen daisy chain loops 13.

[019] According to the present invention, the sectioned edge card connector 14 couples each one of the positively biased gangs 30 to the electrical measuring device 26. In contrast, the shorted edge card connector 16 electrically shorts each of the negatively biased gangs 32 together to form one common negatively biased gang 34, and couples the common negatively biased gang 34 to the electrical measuring device 26. During testing, the electrical measuring device 26 indicates whether there is any leakage between one or more of the positively biased gangs 30 and the common negatively biased gang 34.

[020] If the electrical measuring device 26 does not indicate a leak is present, then the leakage test ends. Approximately 90% or more of all test packages 18 should pass the leakage test. If the electrical measuring device 26 does indicate a leak is present, then the presence of the leak is confirmed by switching positions of the edge card connectors 14 and 16 on the gang testing board 12. The test is then repeated with the positively biased gangs 32 held in common by

the shorted edge card connector 16, and individual negatively biased gangs 34 are input to the electrical measuring device 26 by sectioned edge card connector 14. In an alternative embodiment, the test socket 20 with the test package 18 could be turned around on the gang testing board 12, rather than physically switching the connectors. However, this would require the presence of symmetrical connections.

[021] If a leak is still indicated during the repeated test, then the electrical measuring device 26 identifies the leaking negatively biased gang 34. The use of the gang testing board will not automatically identify the exact failure site. However, this may be accomplished by manually probing to identify which one of the daisy chained loops 13 in the identified gang is leaking, or by ATE testing. In the case where ATE testing is chosen, the present invention eliminates 90% of the samples requiring ATE testing.

[022] Utilizing the reliability system 10 of the present invention, failures can be isolated to the following levels:

- Leak Isolation- Based on 64 contact(32 channel)
    i. For a 2397 pin BGA,13 loops
    ii. For a 1413 pin BGA, 7 loops
    iii. For a 313 pin BGA, 2 loops
- Open Isolation
    i. For a 2397 pin BGA, 50*-25 loops
    ii. For a 1413 pin BGA, 27*-14 loops *Kelvin Measurement.

[023] The reliability testing system using daisy chain gang testing in accordance with the present invention provides the following advantages; 1) reduced cost, 2) faster test turnaround, 3) can be used for real time testing, such as during drying of the test packages in an oven, and 4) testing can be performed at sites where an ATE tester is not readily available.

[024] In an alternative embodiment, a gang testing board for leakage testing may be constructed with edge card connectors on all four sides. FIG. 3 is a diagram illustrating a gang testing board having four edge card connectors (A), (B), (C), and (D), thereby decreasing the number of daisy chain loops in each gang. By using electrical measuring device 26, such as a simple 32 channel data logger, for instance, the leakage testing can proceed as follows:

[025] In this embodiment, edge card connector (A) is a shorted edge card connectors that shorts together all negatively biased gangs, while the other three edge card connectors (B), (C), and (D) each coupled to respective positively biased gangs of loops. With edge card connector (A), 32 parallel paths are created, each with 1/32 of one side of the I/O loops, where, all of the Vss loops are held common.

[026] For leak test measurements of I/O, measurements are taken with edge card connector (A). If there is no leaking, then I/O loop testing is complete. If a leak exists then the above test is repeated with edge card connector (A) used to short the positively biased gangs and edge card connectors (B), (C), and (D) coupled to respectively negatively biased gangs. This will allow identification of

the exact negative to positive biased gang location. For leak measurement of I/O to planes, each Vdd plane is represented as a connection finger of the positive biased sectioned edge card connector, while each Vss plane is represented as a connection finger of the negatively biased sectioned edge card connector to determine if the I/O is leaking across the plane isolation rings.

[027] In a further embodiment, depending on the application, two of the four edge card connectors could be shorted edge card connectors, while the other two are sectioned.

[028] The use of a shorting edge card connector to allow selective edge card connections on all four board sides has the ability to isolate faults with a relatively small number of loops per gang. Without the shorting edge card connector technique, many more multiples of single edge card connectors or a sophisticated ATE would be needed to accomplish the same level of isolation. Thus, the present invention provides the ability to approach the isolation achieved with expensive Automated Test Equipment using equipment costing several orders of magnitude less.

[029] A reliability testing system using daisy chain gang testing has been disclosed. The present invention has been described in accordance with the embodiments shown, and one of ordinary skill in the art will readily recognize that there could be variations to the embodiments, and any variations would be within the spirit and scope of the present invention. Accordingly, many

modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.